Design & Analysis of Low Leakage 64-Bit Hybrid Adder using 22nm Technology

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***Abstract*— Adders are one of the basic components in most of the digital systems. Optimization of these adders can improve the performance of the entire system. In this paper we present a multiplexer based hybrid adder to reduce leakage power. To reduce the leakage power we have used the transistor stacking technique. We have compared the conventional multi-level adder and hybrid adder in terms of delay, average power, leakage power and PDP. All the simulations are done using Tanner Tool v13.0 at 500MHz frequency in 22nm technology at a supply voltage of 1.0V. Simulation results show the decrease of leakage power in hybrid adder.**

Keywords*—HAU (Hybrid Adder Unit), CLA (Carry Look Ahead Adder), CSA (Carry Skip Adder), CMOS (Complementary metal oxide semiconductor), VLSI (Very large scale integration), PDP (Power delay product).

I. INTRODUCTION

Adders are key building block in arithmetic and logic units(ALU) and hence increasing their speed and reducing their power/energy consumption strongly affect the speed and power consumption of processors. Obviously, it is highly desirable to achieve higher speeds at low power/energy consumption, which is a challenge for the designers of general purpose processors [2]. Several adder implementations, including ripple carry, Manchester carry chain, carry skip, carry look ahead, carry select, conditional sum and various parallel prefix adders are available to satisfy different area, delay and power requirements. The ripple carry adder(RCA) is the simplest adder, but has the longest delay because every sum output needs to wait for the carry-in from the previous adder cell. It uses O(n) area and has a delay of O(n) for a n-bit adder.

The carry look ahead adder has delay O(log*n*) and uses O(*n*log*n*) area. Carry Skip Adders(CSA) also dissipate less power than other adders due to their low transistor counts and short wire lengths. Existing fast adders include carry look ahead adder(CLA), carry skip adder(CSA) and conditional sum adder. The simplest adder architecture is the Ripple Carry Adder. In this adder, every block computes a 1bit sum and provide the resulting output and the carry bit for next 1bit adder. For this adder the worst case delay increases linearly with the number of bits. So, this adder is not very efficient when large number bit numbers are used. Many times critical applications uses carry look ahead schemes(CLA) to derive a fast but high area adder.[1]

The Carry Skip Adder(CSA) provides a compromise between ripple carry adder and CLA adder. The carry skip adder divided the words to be added into blocks. Within each block ripple carry is used to produce the sum bit and the carry. When the carry of first block is generated, the succeeding carries are generated with two gate delays per block. Hence, the second block waits until the first ripple carry block generates a carry. [1]

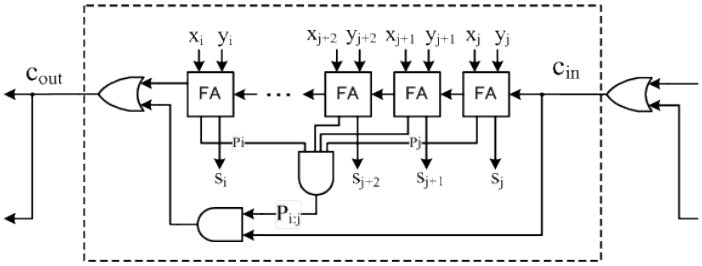

Fig.1 Block Diagram of Carry Skip Adder [1]

In this paper we have presented a low leakage multiplexer based hybrid adder. The hybrid adder combine both carry look ahead and multiplexer based carry skip architectures to speed up its performance [7]. The decrease in leakage power is being achieved by using stacking technique.

Both conventional and hybrid adders are compared in terms of delay, leakage power, average power and PDP, with and without using stacking technique. The rest of the paper is organized as follows: Section II, present our proposed designs. In Section III, simulation results are shown. Finally Section IV contains a conclusion.

II. CONVENTIONAL CLA DESIGN

A carry-lookahead adder improves speed by reducing the amount of time required to determine carry bits. Unlike the Ripple Carry Adder for which the carry bit is calculated alongside the sum bit, and each bit must wait until the previous carry has been calculated. The CLA calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits. The Kogge-Stone adder and Brent-Kung adder are examples of this type of adder.

Let the two numbers to be added are a_i and b_i. The basic architecture of fast adders, produces the carry generate function G_i and the propagation function P_i.

$$Gi = ai \bullet bi \text{ and } Pi = ai \oplus bi \quad (1)$$

The conventional CLA consists of a PG-unit, a CLA unit, and a summation unit. The summation unit and carry bits are generated as follows (2-4),

$$Sum_i = P_i \oplus C_{i-1} \text{ and } C_i = G_i + P_i \bullet C_{i-1} \quad (2)$$

The carry-lookahead unit is realized by the 4-bit CLA (CLA-4) and 4-bit block CLA (BCLA-4), as shown in Fig. 2.1 and Fig. 2.2. By (2), the carry outputs C_0, C_1, C_2, and C_3 are expressed as follows,

$$C_0 = G_0 + P_0 C_{-1}$$

$$C_1 = G_1 + G_0P_1 + P_1P_0C_{-1} \quad (3)$$

$$C_2 = G_2 + G_1P_2 + G_0P_2P_1 + P_2P_1P_0C_{-1}$$

$$C_3=G_3 + G_2P_3+G_1P_3P_2+G_0P_3P_2P_1+ P_3P_2P_1P_0C_{-1}$$

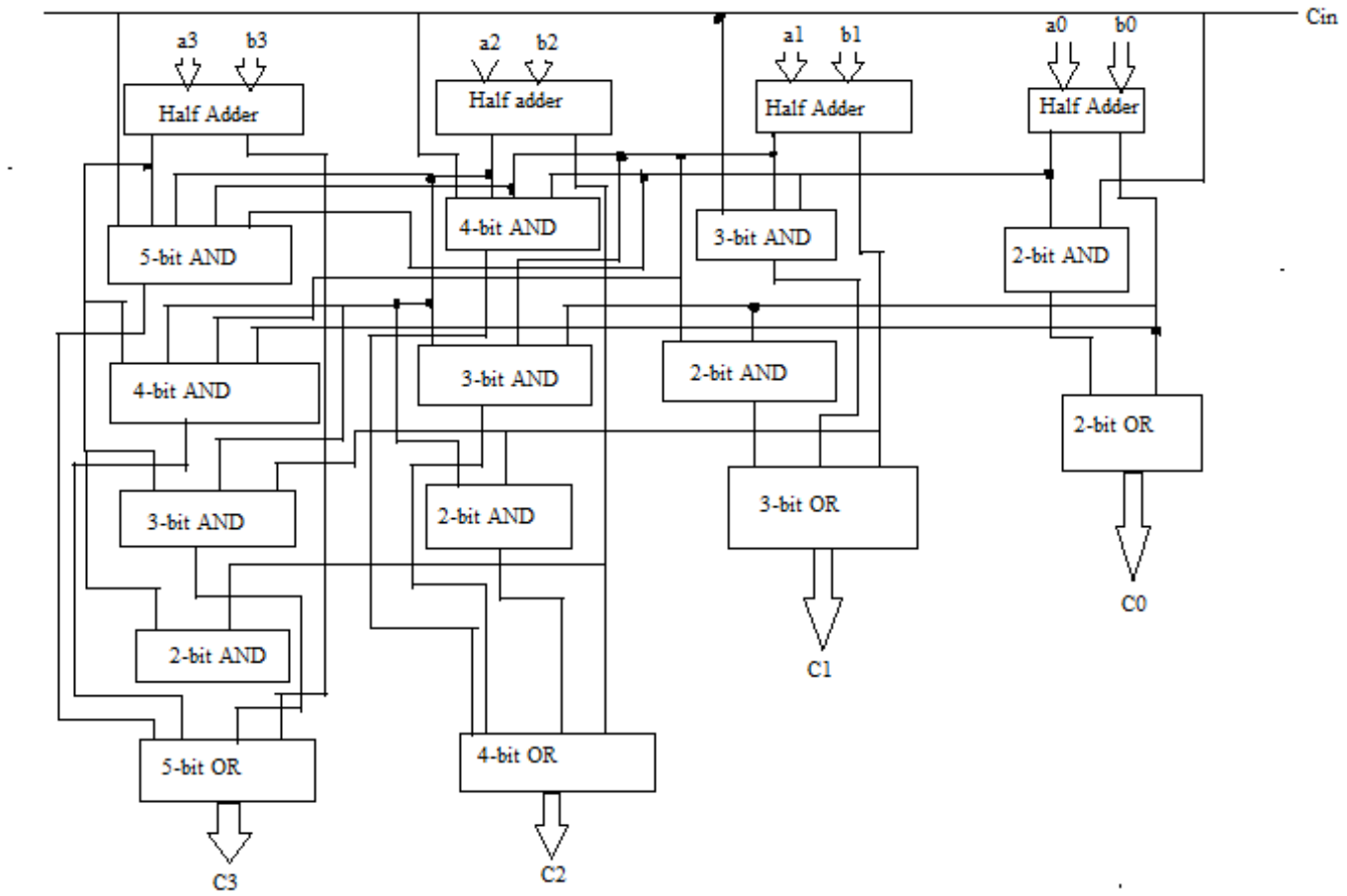

Fig.2.1 Block diagram of 4-bit CLA [7]

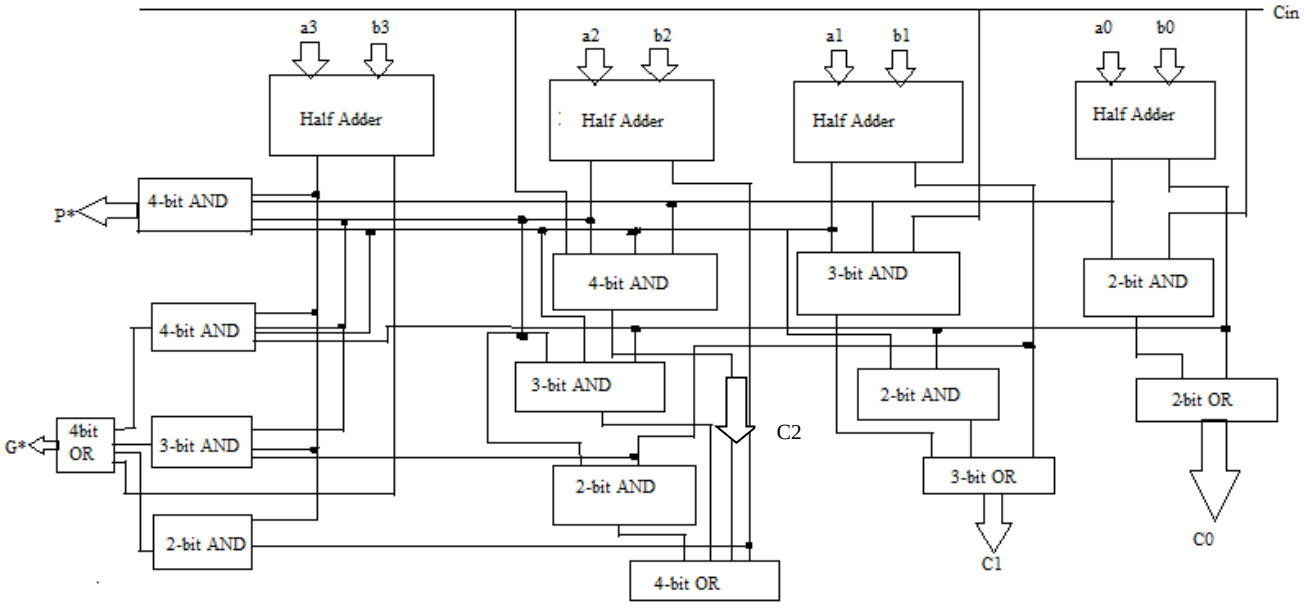

Fig.2.2 Block diagram of 4-bit BCLA [7]

Similarly, the carry outputs, C_0, C_1, and C_2, of BCLA-4 are the same as those in (3), and the group propagate function P* and group generate function G* are expressed as,

$$P^* = P_3P_2P_1P_0 \text{ and } G^* = G_3 + G_2P_3 + G_1P_3P_2 + G_0P_3P_2P_1 \quad (4)$$

Multilevel 64bit CLA comprised of four CLA-4 unit and 16 BCLA-4 units. [7]

III. HYBRID ADDER ARCHITECTURE

Let P' denote as the bit-complement of P. The carry outputs in (3) can be written as:

$$C_0 = G_0P_0' + P_0C_{-1}$$

$$C_1 = (G_1 + G_0P_1)(P_1P_0)' + P_1P_0C_{-1} \quad (5)$$

$$C_2 = (G_2 + G_1P_2 + G_0P_2P_1)(P_2P_1P_0)' + P_2P_1P_0C_{-1}$$

$$C_3 = (G_3+G_2P_3+G_1P_3P_2+ G_0P_3P_2P_1)(P_3P_2P_1P_0)'+P_3P_2P_1P_0C_{-1}$$

Property 1.

Let,

$$P_0\# = P_0;\ P_1\# = P_1P_0,\ P_2\# = P_2P_1P_0\ ;\ P_3\# = P_3P_2P_1P_0 = P3^* \quad (6)$$

$$G_0\# = G_0;$$

$$G_1\# = G_1 + G_0P_1,$$

$$G_2\# = G_2 + G_1P_2 + G_0P_2P_1,$$

$$G_3\# = G_3+G_2P_3 + G_1P_3P_2 + G_0P_3P_2P_1 = G3^*$$

and let MUX(a, b;x) denote as the multiplexer that outputs a if x=0 or b otherwise. [7]

The Hybrid Adder Unit-4bit is comprised of three parts as shown in (a) Carry-lookahead unit (CLU), (b) MUX based Carry skip unit, (c) Input carry. A CLU takes in the Carry propagate functions Pi's and carry generate functions Gi's as inputs and produces the functions G3# and P3#. [7]

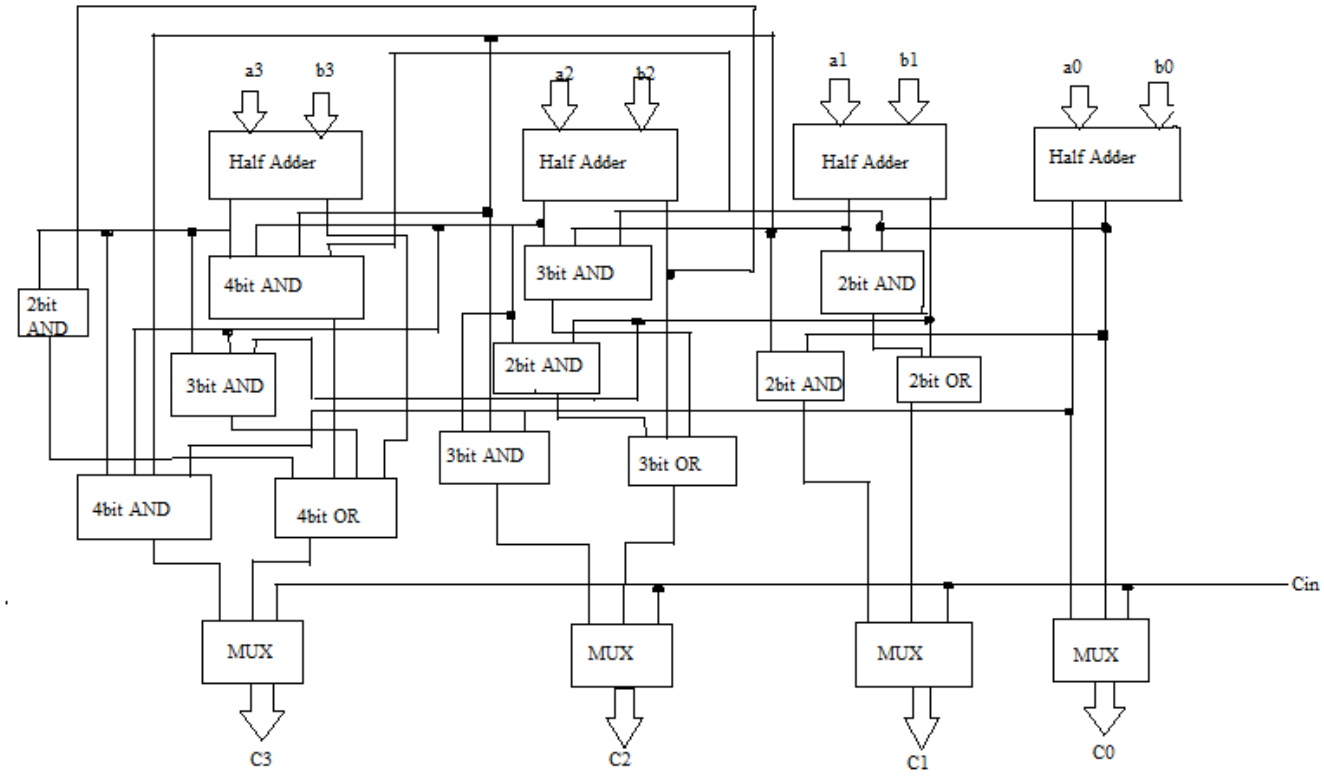

Fig.3.1 Block diagram of 4-bit HAU [7]

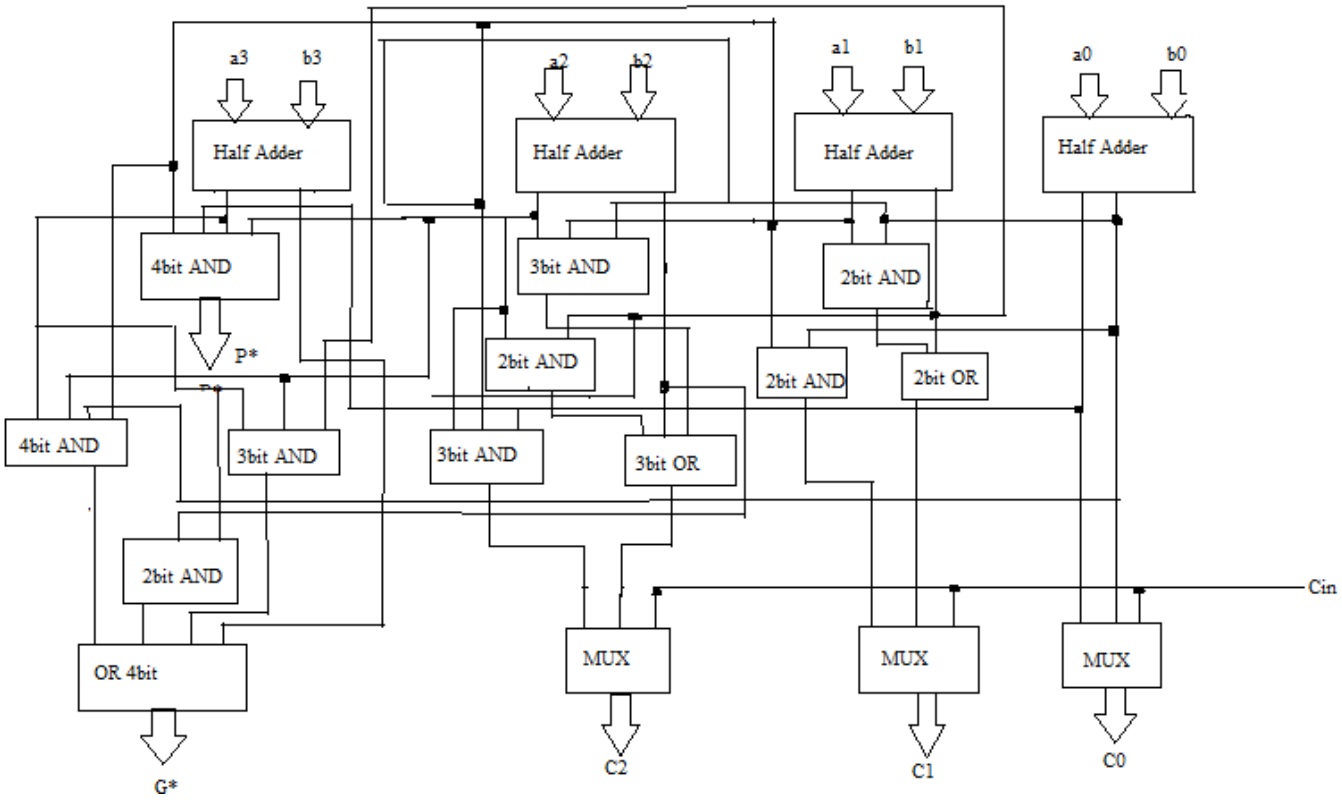

Fig.3.2 Block diagram of 4-bit BHAU [7]

64-bit HAU comprised of four HAU-4 units and 16 BCLA-4 units. [7]

IV. HYBRID AND CONVENTIONAL DESIGN USING STACKING TECHNIQUE

Researchers had presented various leakage power reduction techniques at different levels of design abstraction. [8]

Transistor Stacking: Stack effect is the phenomenon where leakage current decrease due to two or more series transistors that are off. In some circuits, transistor stacking already exists such as NAND gate. In those circuits, where natural stacking does not exist the fore stacking is done by replacing a single transistor width W by two transistors in series each of width W/2. [8]

This concept of stacking technique has been applied to both the conventional adder design and the hybrid adder design in order to obtain low leakage.

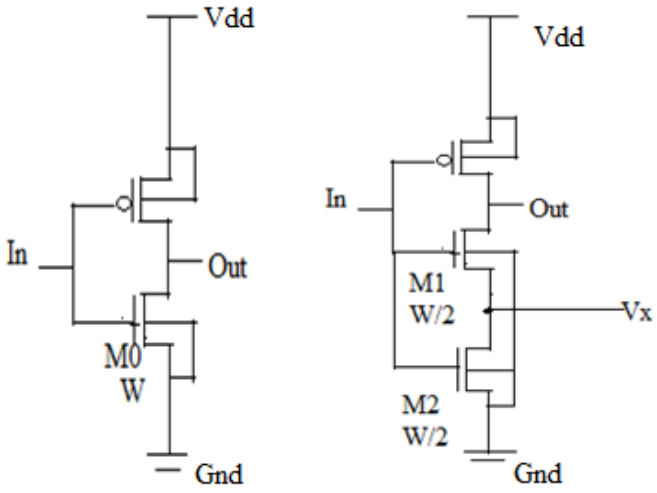

Fig.4 Transistor Stacking

Standard CMOS Inverter [5] CMOS Inverter after force stacking [8]

V. SIMULATION RESULTS

Conventional CLA design and the multiplexer hybrid adder design is compared in terms of area, delay, PDP, average power and leakage power. The stacking technique has been used in order to achieve the low leakage . The leakage power of the adder designs are compared with and without stacking. All the simulations are performed at 22nm technology, 1V power supply at frequency of 500MHz. All circuit logic style is designed using different gate width of NMOS and PMOS and with a minimum length of 22nm for NMOS and PMOS by using Tanner V13 Tool and TSPICE tool. The output signal waveform for 4-bit and 64-bit hybrid adders at power supply of 1.0v is shown in Fig 5(a)-5(b).

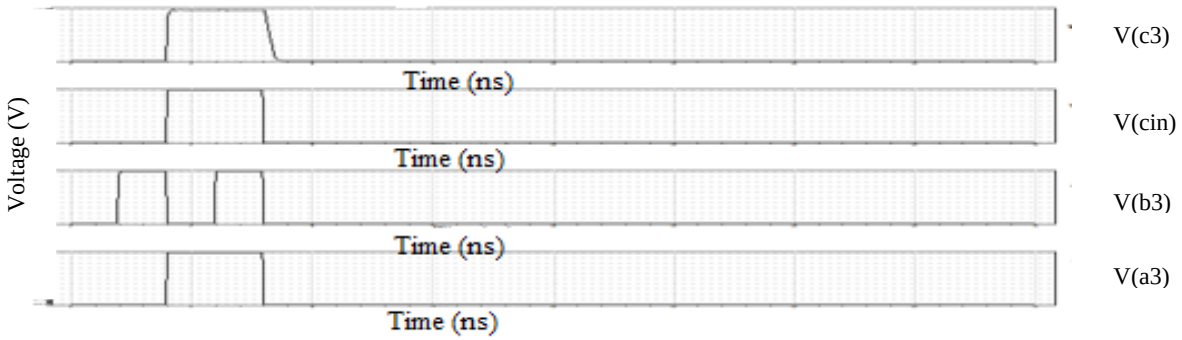

Fig. 5(a) Simulation waveform of 4-bit Hybrid Adder

The results of 64-bit proposed adders are shown in Table I at 1.0v supply voltage and 500MHz frequency. Result shows that stacked Hybrid adder has 44.72% lower leakage power as compared to non-stacked hybrid adder. It has 11.76% improvement in average power dissipation. Although, there is a slight increase in delay of hybrid adders as a result of stacking. Also the conventional CLA circuit consume 25.18% less average power by using the stacking technique and sho 51.12% reduction in leakage power. Fig.6 shows the comparison of leakage power and average power consumption of 64-bit Hybrid adder and Conventional Carry lookahead adder.

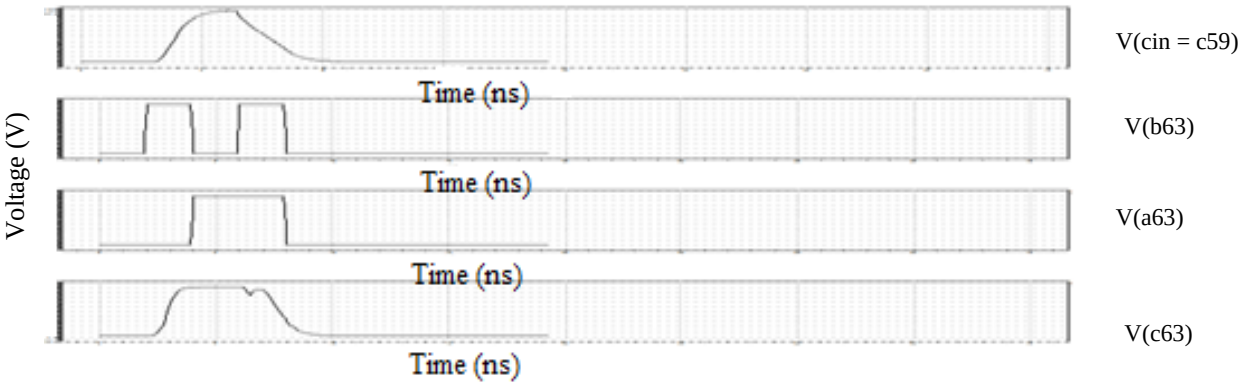

Fig. 5(b) Simulation waveform of 64-bit Hybrid Adder

TABLE I: Comparison of 64-bit Hybrid adder and CLA at 1.0v and 500MHz frequency

Type of adder	Average Power(µW)	Delay (ns)	Leakage Power (µW)
Conv. CLA	818	4.086	730.50
Hybrid Adder	694.36	0.696	444.04
Stacked CLA	612	6.38	357
Stacked HAU	612.70	1.44	245.43

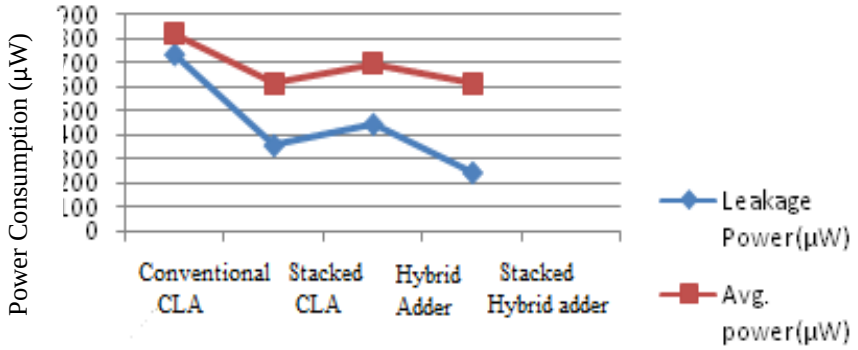

Fig. 6 Comparison of leakage and average power consumption of 64-bit Hybrid adder & CLA

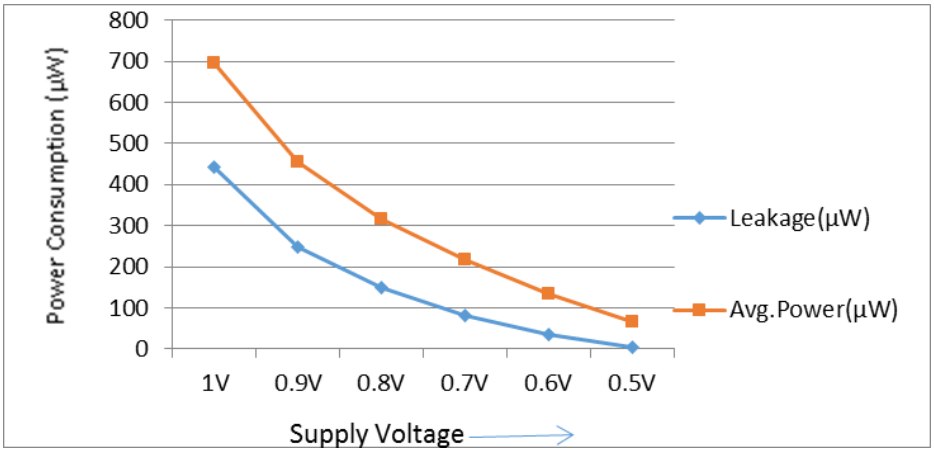

Fig. 7 Power vs. Supply voltage for 64-bit HAU

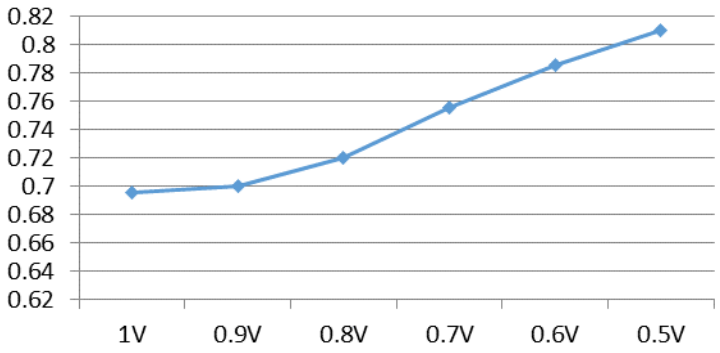

Fig.8 Delay vs. supply voltage for 64-bit HAU

The power consumption corresponding to supply voltages is shown in Fig. 7. The power exponentially reduces as the supply voltage reduces. Fig. 8 shows that the adder has maximum delay of 0.7ns at 1V. The delay linearly increases as supply voltage reduces from 1.0V to 0.5V. This happens because the adder is now operating in subthreshold region, in which the transistor threshold voltage becomes large compared to the supply voltage so that the circuit speed is much slow.

VI. CONCLUSION

64-bit hybrid adder at 22nm technology is designed in this paper. Hybrid architecture is designed using CLA and CSA combined to speed up the performance. To optimize the leakage power, the stacking technique is implemented in 4-bit, 16-bit, 32-bit and 64-bit hybrid adder. Results show that there is 11.76% improvement in average power and 44.72% improvement in leakage power. According to the result, it is concluded that hybrid adder is the best option for advanced low power VLSI arithmetic applications.

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